REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow.

In the May 6, 2005, Office Action in this application, the Examiner objected to the drawings and, in particular, to original Figs. 1A and 3A. Specifically, the Examiner stated that the arrows of the bodies of transistors 102, 104 and 202 should point in instead of out.

On October 12, 2005, Applicant filed corrected replacement drawings to meet the objection stated by the Examiner. A copy of the corrected replacement drawings submission is enclosed herewith.

The Examiner also objected to claim 1, stating that in lines 6, 8, 9 and 12, "cascaded" should be changed to "cascoded".

As indicated above, claim 1 has been amended to meet the Examiner's objections.

Furthermore, the Examiner stated that claim 1 would be allowed if amended to address the Examiner's objections. Therefore, it is believed that claim 1 is now in condition for allowance.

The Examiner rejected claim 2 under 35 U.S.C. 102(b) as being anticipated by the Thomson et al. '502 patent.

Specifically, the Examiner stated that Fig. 4 of the Thomson et al. reference discloses a circuit that includes a resistive divider comprising a first resistor R2 and second resistor R1. The Examiner also states that Fig. 4 of the Thomson et al. reference shows an NMOS transistor 28 having its drain 38 connected to the positive supply voltage Vdd and its source 40 connected to the negative supply V. The Examiner states that the gate 32 of the NMOS transistor 28 is connected to the resistor divider common node and that a capacitor structure C1 is disposed between the source of the NMOS transistor 28 and the positive voltage supply Vdd.

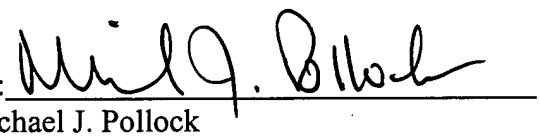
Upon review of Fig. 4 of the Thomson et al. reference, Applicant submits that Fig. 4 shows the capacitor C1 connected between the gate of the NMOS transistor 28 and the negative voltage supply V-. Furthermore, the source region 40 of the NMOS transistor 28 is also connected to the negative voltage supply V- such that the capacitor C1 is connected between the source region 40 and gate electrode of the NMOS transistor 28. This is unlike the time-driver circuit structure recited in claim 2, wherein the capacitor structure is disposed between the source of the NMOS transistor and the positive supply voltage.

For the reasons set forth above, Applicant submits that all claims now present in this application, including newly-added dependent claim 3, which depends from amended claim 1, and newly-added dependent claim 4, which depends from claim 2, patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

STALLMAN & POLLOCK LLP

Dated: October 24, 2005

By: 
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